SEYEDRAMIN RASOULINEZHAD

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RESEARCH INTERESTS

Computer Architectures **FPGA/GPU-based Systems** **Embedded Systems**

EXPERIENCES

Associate Researcher, GPU DDK team July 2021 - Up to now
Hisilicon, Huawei Technologies, Edmonton, Canada

EDUCATION

Doctor of Philosophy in Engineering & IT July 2018 - Up to now
School of Electrical & Information Eng., University of Sydney, Sydney, Australia. Supervisor: Prof. Philip Leong

Bachelor of Science in Electrical Engineering (Major: Digital Systems) August 2012 - June 2017
EE Department of Sharif University of Technology, Tehran, Iran. (GPA 17.08/20 - 152 credits)

Diploma in Mathematics and physics August 2008 - June 2012
Allameh Helli, Tehran - NODET (National Organization for Development of Exceptional Talents) GPA: 19.1/20.0

PUBLICATIONS

- **Rethinking Embedded Blocks for Machine Learning Applications**
Seyedramin Rasoulinezhad, Esther Roorda, Steve Wilton, Philip H. W. Leong, David Boland, **ACM TRETS21**
To explore new FPGA embedded block design spaces in a methodical manner, we first propose a problem formulation, which covers many basic linear algebra primitives and DNN kernels. This leads to a quantitative methodology for deriving efficient coarse-grained compute block architectures from benchmarks. Partially published in: **MLBlocks: FPGA Blocks for Machine Learning Applications** SeyedRamin Rasoulinezhad, David Boland, Philip H.W. Leong, **FPGA21**

- **FPGA Architecture Exploration for DNN Acceleration**
Esther Roorda, Seyedramin Rasoulinezhad, Philip H. W. Leong, Steve Wilton, **ACM TRETS22**
We present an open-source benchmark circuit generator that creates realistic DNN-oriented circuits for use in FPGA architecture studies.

- **Applications and Techniques for Fast Machine Learning in Science**
By 47 authors including me, **Frontier in Big Data-2022**
It's a review report discussing integration of ML into the real-time data processing loop to accelerate scientific discovery.

- **NITI: Training Integer Neural Networks Using Integer-Only Arithmetic**
Maolin Wang, Seyedramin Rasoulinezhad; Philip H. W. Leong; Hayden K.H. So, **IEEE TPDS22**
We present a novel NN training framework called NITI that exclusively utilizes low bitwidth integer arithmetic. Particularly, NITI stores all parameters and accumulates intermediate values as 8-bit integers while using no more than 5 bits for gradients.

- **APIR-DSP: An approximate PIR-DSP architecture for error-tolerant applications**
Yuan Dai, Simin Liu, Yao Lu, Hao Zhou, SeyedRamin Rasoulinezhad, Philip H.W. Leong, Lingli Wang, **FPT21**
We upgrade the performance of the previously proposed PIR-DSP block with approximate computing techniques

- **A Block Minifloat Representation for Training Deep Neural Networks**
Sean Fox, SeyedRamin Rasoulinezhad, Julian Faraone, David Boland, Philip H.W. Leong, **ICLR21**
We introduce Block Minifloat (BM), a new spectrum of minifloat formats capable of training DNNs end-to-end with only 4-8 bit weight, activation and gradient tensors.

- **LUXOR: An FPGA Logic Cell Architecture for Efficient Compressor Tree Implementations**
SeyedRamin Rasoulinezhad, Siddhartha, Hao Zhou, Lingli Wang, David Boland, Philip H.W. Leong, **FPGA20**
We propose two tiers of modifications (vendor-agnostic and vendor-specific) to FPGA logic cell architecture to deliver a variety of performance and utilization benefits, targeting compressor trees, with only minor area overheads.

- **MajorityNets: BNNs Utilising Approximate Popcount for Improved Efficiency**
SeyedRamin Rasoulinezhad, Sean Fox, Hao Zhou, Lingli Wang, David Boland, Philip H.W. Leong, **FPT19**
We proposed an approximation to XnorPopcount for BNNs, called XNorMaj operation, based on integration of XNOR, Majority, and popcount circuits which is inspired by FPGA LUT schemes.

- **PIR-DSP: An FPGA DSP block Architecture for Multi-Precision Deep Neural Networks**
SeyedRamin Rasoulinezhad, Hao Zhou, Lingli Wang, Philip H.W. Leong, **FCCM19**
We proposed new FPGA DSP block, called PIR-DSP, which incorporates precision, interconnect and reuse optimisations to better support 2-dimensional low-precision DNN applications.

- **Prediction of LifeThreatening Heart Arrhythmias Using Obstructive Sleep Apnoea Characteristic**
Ghazaleh Mohammad Alinejad, SeyedRamin Rasoulinezhad, Mohammad Bagher Shamsollahi, **ICEE19**
We presented a algorithm to predict heart arrhythmias based on new feature set inspired by conventional sleep apnoea detection features.

PATENTS

- **"Logic cell architecture"**, Australian Provisional Patent Application No. 2020900509, International Patent Application No PCT/AU2021/050148, filed by The University of Sydney
- **"An improved hardware primitive for implementations of Deep Neural Networks"**, PCT Patent Application No. PCT/AU2020/050395, filed by The University of Sydney

RESEARCH EXPERIENCE

- **Efficient FPGA Architectures for Machine Learning Applications,** Prof. Leong — Jul18 - now
- **Emulating SD simulations on FPGA,** Dr.Hashemi — Feb18 - Jun18
- **Designing SDAccel compatible PCIe-based FPGA board,** Mr.Dehdast — Aug17 - Feb18
- **Smart In-Sole Gadget,** Communication via BluetoothLE, Dr.Shabany & Dr.Hashemi — Jun15 - Jun17
- **Blood pressure & Heart rate Gadget,** Dr.Shabany — Jun16 - May17
- **PID & Fuzzy Controller on Prostate FNA needle System,** Dr.Jahed — Sep14 - Jun18

HONORS AND AWARDS

- 3rd/19K, the National Entrance Exam of the Public Universities (Iran) for M.S. Computer Architecture — 2018
- 4th place among Iranian students in 11th Microelectronics Olympiads of Armenia - Synopsys `iceep.ir` — 2016
- 1st place in Sharif FPGA competition - TRAX Game - `fpga.sharif.ir` — 2016
- 3rd place in Sharif cup III - Explorer Robot - `sharifcup.sharif.ir` — 2014
- 1st place in Sharif cup II - Multi-Robot Task - `sharifcup.sharif.ir` — 2013
- 42nd/230K, The National Entrance Exam of the Public Universities of Iran, Physics and Mathematics — 2012
- Membership of Iranian National Elites Foundation — 2012

INTERNSHIP EXPERIENCES

- Lab lecturer of Vivado Suite Workshops at **"DDDS"** Center (number 304 at Sharif University of Technology services Complex) (Manager: Dr. Mehdi Shabany) Website: `ddds.sharif.ir` — Jul16 - Jun18
- Part time researcher at **"Matin Technology Center"**, Health Gadget, Company at 1st Roshd Center, Sharif University of Technology. (Manager: Dr. Mehdi Shabany) — Jul15 - Jun18
- Part time researcher at **"Rizpardazesh"** company (Number 101 at Sharif University of Technology services complex) (Manager: Dr. Bijan Vosoughi Vahdat) `odmt.sharif.ir` — Feb14 - Mar15

SELECTED COURSE PROJECTS

- **Implementing DVBT (full ASIC flow, 90nm), Digital VLSI Architecture, Dr.Shabany**
- **Implementing PHY module of Protocol 802.11a (full ASIC flow, 90nm), VLSI, Dr.Shabany**
- **Implementing JPEG Protocol (full ASIC flow, 90nm), Designing ASIC/FPGA Systems, Dr.Shabany**
- **Implementing a Super-scalar MIPS uP, Advanced Computer Arch., Dr.Movahedin**
- Movement Recognition from EEG Signals, Artificial Intelligence, Dr.Hajipour

- Simple Counter Strike-like game using OpenGL and C++, Computer Interface Circuits, Dr.Movahedin
- Audio Recorder with Voice Filtering & Echo by NIOS II, Embedded Systems, Dr.Alizadeh
- Simple Telecommunication App by Android, Data Networks, Dr.Pakravan
- Sound Recorder (by Cortex-M3 ARM board & PC-MatLab), Microprocessor System Design I, Dr.Sanae
- Wending Machine (combine AVR & 8051 & PC Serial Connection), Computer&Microprocessor Arch., Dr.Jahed
- Snake Game (Multi-thread), Advanced Programming ● 2D Football, C++, Introduction to Programming

TEACHING EXPERIENCES

- Lab demonstrator, Computer Architecture, Prof. Philip Leong — 18S2, 19S2
- Lab demonstrator, Digital Logic, Dr. David Boland — 19S1
- Head & Teaching Assistant, Advanced ASIC/FPGA Lab, Dr.Shabany (3 semesters) — F16, S17, F17
- Head Assistant, Microprocessor & and Computer Arch., Dr.Hashemi (2 semesters) — S16, S17
- Head & Teaching Assistant, Logic System Design, Dr.Tabandeh (4 semesters) — F15, S16, F16, S17
- Teaching Assistant, Computer & Microprocessor Architecture, Dr.Tabandeh (1 semester) — S15
- Teaching & Lab Assistant, FPGA/ASIC Systems & Logic circuits, Dr.Shabany (3 semesters) — S15, S16, S17
- Teaching Assistant, Microprocessor System Design II, Dr.Saleh (1 semester) — S16
- Teaching & Lab Assistant, Microprocessor & and Computer Arch., Dr.Bagheri (3 semesters) — F14, F15, F16
- Teaching Assistant, Microprocessor & and Computer Arch., Dr.Jahed (1 semester) — F14

ACTIVITY

- **Shadow PC member, EuroSys 2021, ACM, Edinburgh, UK — 2020**
- **Reviewer, IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II) — 2020 - now**
- **Member of The Center for Spatial Computational Learning - `spatialml.net`, — 2020 - now**
- **Digital support, HDR Student Connect-19, The University of Sydney — 2019**
- **Reviewer, ACM Transactions on Reconfigurable Technology and Systems (TRETS) — 2018 - now**
- **Reviewer, IEEE Transactions on Computer-Aided Design (TCAD) — 2018 - now**
- **Project Manager at "Connected Cars Live Demo" as a 5G Application in Smart Cities, Iran TeleCom Fair 2017, MCI Co., Dr.Khalaj, `irantelecomfair.com` — Oct17**
- Supervisor of Microprocessor Lab, Dr.Hashemi, `microlab.ee.sharif.edu` — 2015-18
- Member of Robotic & Machine Vision Lab, Dr.Jahed — 2014-18
- Editing "Microprocessor & Computer Arch." Book, Sharif University of Tech. Publication, Dr.Tabandeh — 2014
- 2nd and 3rd Sharif cup Technical Committee — 2013 and 2014
- Lecturing at Sharif cup Summer Robotics Workshop — 2014
- Editing "3rd Ed. Calculus for Senior High school Student" Book, Fatemi Publications, Dr. Khakpash — 2011

TUTORIAL CERTIFICATIONS

Implementation of Embedded systems on Altera FPGAs, By ICCEP, University of Tehran — Sep15
Effective implementation of digital designs by PlanAhead suite, By DDDS — Aug15
Effective imp. of digital designs on Xilinx FPGA - Intermediate&Advanced, By DDDS — Sep&Aug14

SKILLS

ASIC/FPGA: SDAccel (Xilinx), ASIC-90nm design flow (Synopsys Design Compiler, Cadence SOC Encounter), FPGA design flow (Vivado Design Suite & HLS tool, ModelSim, ISE, QuartusII), Hardware Language: Verilog HDL & VHDL and Familiar with FPGA boards (DE2 Board, Intel & Atlys Board, Xilinx), HSpice
Embedded System: Implementing Embedded Microcontroller NIOS II, ARM-C (especially on Cortex-M0, M3), Assembly(X86), Arduino-based Embedded Systems, Controlling system by ATmega & ATtiny IC families
Robotics: PCB designing by Altium Designer, Mechanical Designing like Corel & AutoCad
Programming Languages: Python (DNN implementation using PyTorch/TensorFlow), C/C++, OpenGL, Vulkan, Android, MATLAB, **Parallel Programming:** CUDA, Pthread*, MPI*, OpenCL, OpenCV
OS: Windows, Linux (CentOS, Ubuntu, Embedded Linux like Raspbian*) *** Basic Knowledge**

REFERENCES

Prof. Leong (Supervisor)

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Dept. of Electrical Engineering
University of Sydney
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Dr. David Boland (Co-supervisor)

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